"BIG BOARD II"

4 MHz Z80-A SINGLE BOARD COMPUTER WITH "SASI" HARD-DISK INTERFACE

CAL-TEX COMPUTERS, INC.

780 E. TRIMBLE ROAD #504 • SAN JOSE. CA 95131 • (408) 942-1424

NEW LOWER PRICES! ***NOW IN "UNKIT"* FORM TOO!***

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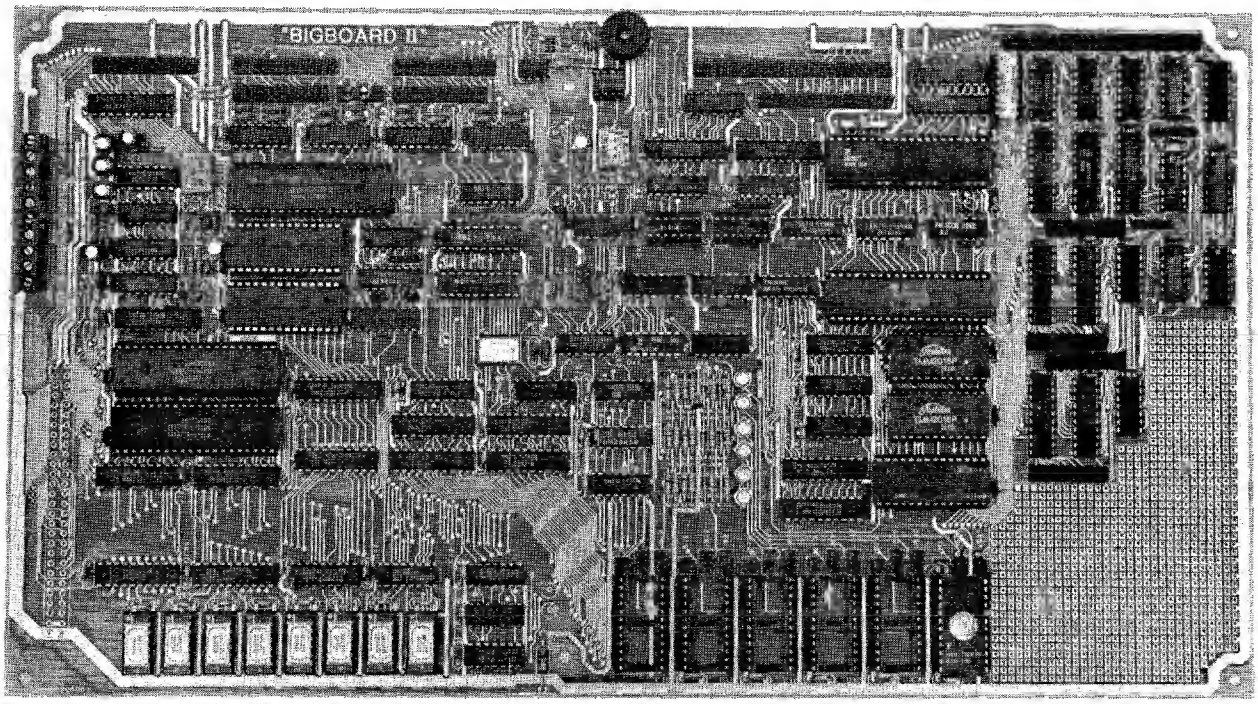
4 MHz Z80-A SINGLE BOARD COMPUTER WITH "SASI" HARD-DISK INTERFACE



$795 ASSEMBLED & TESTED $545 "UNKIT"* $245 PC BOARD WITH 16 PARTS

Jim Ferguson, the designer of the "Big Board" distributed by Digital Research Computers, has produced a stunning new computer that Cal-Tex Computers has been shipping for a year. Called "Big Board II", it has the following features:

■ 4 MHz Z80-A CPU and Peripheral Chips

The new Ferguson computar runs at 4 MHz. Its Monitor code is lean, uses Mode 2 intarrupts, and makes good use of the Z80-A DMA chip.

■ 64K Dynamic RAM + 4K Static CRT RAM + 24K E(E)PROM or Static RAM

"Big Board II" has three memory banks. The first memory bank has eight 4164 DRAMs that provide 60K of user spaca and 4K of monitor space. The second memory bank has two 2Kx8 SRAMs for the memory-mapped CRT display and space for six 2732As, 2Kx8 static RAMs, or pin-compatible EEPROMS. The third memory bank is for RAM or ROM added to the board via the STD bus. Whether bought as a bare board, an "unkit"*, or assemblad and tasted, it comas with a 2732 EPROM containing Russell Smith's superb Monitor.

■ Multiple-Density Controller for SS/DS Floppy Disks

The new Cal-Tex single-board computer has a multiple-density disk controllar. It can use 1793 or 8877 controller chips since it generatas tha side signal with TTL parts. The board has two connectors for disk signals, one with 34 pins for 5.25" drives, tha other with 50 pins for 8" drives.

■ Vastly Improved CRT Display

The new Ferguson SBC uses a 6845 CRT controllar and SMC 8002 video attributes controllar to produce a display rivaling the display of quality terminals. There are three display modes: Character, block-graphics, and line-graphics. Tha board amulatas an ADM-31 with 24 lines of 80 characters formed by a 7x9 dot matrix.

■ STD Bus

The new Ferguson computer has an STD Bus port for easy system axpansion.

■ DMA

Tha new Ferguson computar has a Z80-A DMA chip that will allow byte-wise data transfers at 500 KBytes per second and bit-serial transfars via tha Z80-A SIO at 880 Kbits per sacond with minimal processer overhaad. Whan a hard-disc subsystem is added, the DMA chip makes impressive disk performance possible.

SIZE: 8.75" x 15.5"
POWER: +5V @ 3A, +-12V @ 0.1A

■ "SASI" Interface for Winchester Disks

Our "Big Board II" implemants tha Host portion of the "Shugart Associates Systems Interface." Adding a Winchester disk drive is no harder than attaching a floppy-disk drive. A user simply 1) runs a fifty-conductor ribbon cable from a header on the board to a Xebac controllar that costs only $295 and implements the controllar portion of the SASI interface, 2) cables tha controllar to a Saagate Technology ST-506 hard disk or one compatible with it, and 3) provides power for tha controllar-card and drive. Sinca our CBIOS contains coda for communicating with hard-disks, that's all a user has to do to add a Winchester to a system!

■ Two Synchronous/Asynchronous Serlal Ports

With a Z80-A SIO/O and a Z80-A CTC as a baud-rate generator, the new Ferguson computer has two full RS232-C ports. It autobauds on both.

■ A Parallel Keyboard Port + Four Other Parallel Ports for User I/O

The new Cal-Tex single-board computer has one parallel port for an ASCII keyboard and four others for user-defined I/O.

■ Two Z80-A CTCs = Eight Programmable Counters/Timers

The new Ferguson computer has two Z80-A CTCs. One is usad to clock data into and out of the Z80-A SIO/O, whila tha other is for systems and applications use.

■ PROM Programming Circuitry

The new Cal-Tex SBC has circuitry for programming 2716s, 2732(A)s, or pin-compatibla EEPROMs.

■ CP/M 2.2**

CP/M with Russell Smith's CBIOS for the new Cal-Tex computer is available for $150. The CBIOS is available separataly for $25.

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* *The "unkit" is a fully-socketed, wave-soldered "Big Board II". It requires NO soldering. All an "unkit" purchaser must do is carefully insert the prime ICs we supply in the proper sockets and systematically proceed to bring up and test the board.*

***CP/M is a registered trademark of Digital Research.*

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Terms: Orders paid for with a cashier's check or bank card will be shippad within threa working days. Orders paid for with a parsonal check will be shipped within three weeks. Add $5 for packing & shipping in North America.

"BIG BOARD II" ASSEMBLY MANUAL

Preliminary Draft
Subject to Revision

Cal-Tex Computers, Inc
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Boulder Creek, CA 95006
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CONTENTS

"BIG-BOARD II" PARTS LISTED BY NUMBER

SEMICONDUCTORS

Device	Qty	Locations	Comments
Z80-A CPU	1	U39	
Z80-A DMA	1	U62	
Z80-A SIO/O	1	U16	
Z80-A CTC	2	U21,37	
6845(S)	1	U30	Hitachi 6845S preferred.
CRT8002...(SMC)	1	U52	Video attributes controller.

[Use an 8002A with a 16 MHz Video crystal for CRT's with an 18.6 KHz horizontal scan rate, an 8002B-003 with an 11 MHz Video crystal for CRT's with a 15.75 horizontal rate. The display produced by the 8002A is preferable, for its characters are formed by a 7x9 dot matrix and have descenders.]

1793	1	U10	Floppy-disk controller. A Fujitsu MB8877A may be used as well.
FDC9216B (SMC)	1	U6	Floppy-disk data separator.
PAL16L8	1	U23	Proprietary IC. Supplied.
PAL10L8	1	U34	Proprietary IC. Supplied.
2732A	1	U85	250nS Monitor EPROM. Supplied.
4164	8	U72-79	200nS 64K dynamic RAM's without Pin-1 refresh.
TMM2016 or 6116	2	U50,51	200nS 2Kx8 static RAM's.
74LS00	2	U29,31	
74LS02	1	U71,25	
74LS04	5	U19,43,69,91,101	
7406	1	U7	
7407	1	U44	
74LS08	1	U35	
74LS14	1	U17	
74LS30	1	U33	
74LS32	2	U46,97	
7438	3	U88-90	
7445	1	U56	
74LS74	8	U18,22,32,70,92, 100,105,26	
74(LS)86	1	U24	
74LS138	3	U15,27,55	
74LS139	1	U102	
74LS151	1	U12	

74157	1	U42
74LS157	5	U47-49,67,68
74LS164	1	U45
74LS169	1	U36
74LS195	1	U28
74LS240	2	U8,94
74LS244	7	U9,11,38,58,63,64,95
74LS245	6	U40,53,54,61,65,66
74LS259	3	U14,41,96
74LS273	1	U13
74LS373	9	U1,57,59,60,93,98,99,103,104
74LS393	1	U20
555	1	U86
1488	2	U2,4
1489(A)	2	U3,5
2N2222(A)	1	Q1
2N2907(A)	7	Q2-8 Q3,4,5,6,7
1N4148	11	CR1-11 CR6,7,8,9,10

RESISTORS

Single Resistors

1/2 Watt 5%

10 Ohm	1	R38

1/4 Watt 5%

22 Ohm	1	R15
47 Ohm	1	R10
150 Ohm	1	R12
220 Ohm	8	R6,16,24,25,30,31,36,37
680 Ohm	1	R14
1.0 K Ohm	12	R8,9,11,13,18,19,21,23,27,29,33,35
1.2 K Ohm	1	R17
4.7 K Ohm	2	R3,4
10.0 K Ohm	8	R5,7,20,22,26,28,32,34
33.0 K Ohm	2	R1,2

Resistor Networks

6-Pin 10K SIP, Pin 1 Common	2	RN2,3	CTS 750-61-R10K
8-Pin 220/330 Ohm SIP	1	RN1	CTS 750-85-R220/330
16-Pin 220/330 Ohm DIP	1	U87	A/B 316E221331; CTS 761-5-R220/330

CAPACITORS

Disc Ceramic

33 pF	1	C116
150 pF	2	C38,65
300 pF	2	C39,66
390 pF	15	C10-19,111-115
.01 uF	5	C1,2,37,54,59

Bypass Caps.

.1 uF	86	C3-9,22-33,36,40,41,43-53,55-58,60-64,67-110, 117-118

Electrolytic

47 uF 16V	5	C20,21,34,35,42

CRYSTALS

8 MHz	1	Y1
11 MHz		Y2 Use an 11 MHz crystal with a CRT8002B-003, a 16 MHz crystal with a CRT8002A.
16 MHz		Y2

SOCKETS

8-Pin	2	U6,86 -26,
14-Pin	32	U2-5,7,17-20,22,24 29,31-33,35,43-46, 69-71,88-92,97,100-101,105
16-Pin	26	U12,14,15,27,28,36,41,42,47-49,55,56, 67,68,72-79,87,96,102
20-Pin	27	U1,8,9,11,13,23,34,38,40,53,54,57-61, 63-66,93-95,98,99,103,104
24-Pin	8	U50,51,80-85
28-Pin	3	U21,37,52
40-Pin	5	U10,16,30,39,62

CONNECTORS

1x2	2	JB14,15
1x3	4	JB4,8,34,35
1x4	1	JB10+JB11
1x5	2	JB7,9
1x6	1	JB5
2x2	7	JB13,16,19,22,25,28,31
2x3	13	JB17,18,20,21,23,24,26,27,29,30,32,33
2x5	1	JB12
2x6	1	JB2

2x10	4	J8,9,10,11	
2x12	2	JB1,3	
2x13	3	J2-4	
2x17	1	J6	
2x25	2	J5,7	
2x28	1	J1	STD Bus connector. Not supplied.
3x3	1	JB6	Use 1x3 and 2x3 connectors.

MISCELLANEOUS ITEMS
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4-Position DIP switch	1	SW1	CTS 206-4
10-Position Terminal Block	1	TB1	Electrovert 25-104-1053
Beeper	1	DS1	Star-Micronics QMB-06

"BIG-BOARD II" PARTS LISTED BY LOCATION

SEMICONDUCTORS

Location	Device	Comments
U1	74LS373	
U2	1488	
U3	1489(A)	
U4	1488	
U5	1489(A)	
U6	FDC9216B (SMC)	Floppy-disk data separator.
U7	7406	
U8	74LS240	
U9	74LS244	
U10	1793	Floppy-disk controller. A Fujitsu MB8877 may be used as well.
U11	74LS244	
U12	74LS151	
U13	74LS273	
U14	74LS259	
U15	74LS138	
U16	Z80-A SIO/O	Multi-protocol serial i/o chip.
U17	74LS14	
U18	74LS74	
U19	74LS04	
U20	74LS393	
U21	Z80-A CTC	
U22	74LS74	
U23	PAL16L8	Proprietary chip supplied by Cal-Tex Computers.
U24	74(LS)86	
U25	74LS02	
U26	74LS74	
U27	74LS138	
U28	74LS195	
U29	74LS00	
U30	6845(S)	Hitachi enhanced CRT controller chip preferred.
U31	74LS00	
U32	74LS74	
U33	74LS30	
U34	PAL10L8	Proprietary chip supplied by Cal-Tex Computers.
U35	74LS08	
U36	74LS169	
U37	Z80-A CTC	
U38	74LS244	
U39	Z80-A CPU	
U40	74LS245	
U41	74LS259	

U42	74157	
U43	74LS04	
U44	7407	
U45	74LS164	
U46	74LS32	
U47-49	74LS157	
U50,51	TMM2016 or 6116	200 nS 2Kx8 static RAM.
U52	CRT8002...(SMC)	8002B-003 if Y2=11 MHz, 8002A if Y2=16 MHz.
U53,54	74LS245	
U55	74LS138	
U56	7445	
U57	74LS373	
U58	74LS244	
U59,60	74LS373	
U61	74LS245	
U62	Z80-A DMA	
U63,64	74LS244	
U65,66	74LS245	
U67,68	74LS157	
U69	74LS04	
U70	74LS74	
U71	74LS02	
U72-79	4164	200 nS 64K dynamic RAMs without Pin-1 refresh.
U80-84		Users' 2732(A)s, 2Kx8 static RAMs, or EEPROMs.
U85	2732A	250 nS Monitor EPROM. Supplied by Cal-Tex Computers, Inc.
U86	555	Timer.
U87	16-Pin DIP RN 88,89	220/330 Ohm Terminating Resistor Network.
U88-90	7438	
U91	74LS04	
U92	74LS74	
U93	74LS373	
U94	74LS240	
U95	74LS244	
U96	74LS259	
U97	74LS32	
U98,99	74LS373	
U100	74LS74	
U101	74LS04	
U102	74LS139	
U103,104	74LS373	
U105	74LS74	
Q1	2N2222(A)	
Q2-8	2N2907(A)	3--7
CR1-11	1N4148	6,7,8,9,10

RESISTORS

Single Resistors

R1,2	33 K	Unless noted otherwise, the resistors
R3,4	4.7 K	are 1/4 Watt ones with a 5% tolerance.
R5	10 K	
R6	220 Ohms	
R7	10 K	
R8,9	1.0 K	
R10	47 Ohms	
R11	1.0 K	
R12	150 Ohms	
R13	1.0 K	
R14	680 Ohms	
R15	22 Ohms	
R16	220 Ohms	
R17	1.2 K	
R18,19	1.0 K	
~~R20~~	10 K	
R21	1.0 K	
~~R22~~	10 K	
R23	1.0 K	
R24,25	220 Ohms	
~~R26~~	10 K	
R27	1.0 K	
R28	10 K	
R29	1.0 K	
R30,31	220 Ohms	
R32	10 K	
R33	1.0 K	
R34	10 K	
R35	1.0 K	
R36,37	220 Ohms	
R38	10 Ohms	1/2 Watt 5%

Resistor Networks

RN1	8-Pin 220/330 Ohn SIP	CTS 750-85-R220/330
RN2,3	6-Pin 10K SIP, Pin 1 Common.	CTS 750-61-R10K
U87	16-Pin 220/330 Ohm DIP	CTS 761-5-R220/330

CAPACITORS

Capacitors not listed here are not critical. They may be disc ceramic or monolithic providing they have a value of 0.1 uF and a rating of at least 12 Volts.

C1,2	.01	uF	
C10-19	390	pF	
C20,21	47	uF	Electrolytic. Nichicon ULB1C470M preferred.
C34,35	47	uF	Electrolytic. Nichicon ULB1C470M preferred.
C37	.01	uF	
C38	150	pF	
C39	300	pF	
C42	47	uF	Electrolytic. Nichicon ULB1C470M preferred.
C54,59	.01	uF	
C65	150	pF	
C66	300	pF	
C111-115	390	pF	
C116	33	pF	

Connectors

J1	2x28	STD Bus connector
J2	2x13	Parallel keyboard.
J3	2x13	SIO Channel A
J4	2x13	SIO Channel B
J5	2x25	8" Floppy Disk
J6	2x17	5.25" Floppy Disk
J7	2x25	"SASI" Interface
J8	2x10	Parallel Input Port 1
J9	2x10	Parallel Output Port 1
J10	2x10	Parallel Input Port 2
J11	2x10	Parallel Output Port 2
JB1	2x12	SIO Channel A
JB2	2x6	Serial Data Clocks
JB3	2x12	SIO Channel B
JB4	1x3	
JB5	1x6	
JB6	3x3	
JB7	1x5	
JB8	1x3	
JB9	1x5	
JB10+JB11	1x4	
JB12	2x5	Video Output Connector
JB13	2x2	
JB14,15	1x2	
JB16	2x2	

JB17,18	2x3
JB19	2x2
JB20,21	2x3
JB22	2x2
JB23,24	2x3
JB25	2x2
JB26,27	2x3
JB28	2x2
JB29,30	2x3
JB31	2x2
JB32,33	2x3
JB34,35	1x3

ASSEMBLY INSTRUCTIONS

[✓] Carefully inspect the PC board.

[✓] Ascertain that there are no shorts between the power traces and ground.

[✓] Install and solder 40-pin sockets in locations U10, 16, 30, 39, and 62.

[✓] Install and solder 28-pin sockets in locations U21,37, and 52.

[✓] Install and solder 24-pin sockets in locations U50-51 and 80-85.

[✓] Install and solder 20-pin sockets in locations U1, 8-9, 11, 13, 23, 34, 38, 40, 53-54, 57-61, 63-66, 93-95, 98-99, and 103-104.

[✓] Install and solder 16-pin sockets in locations U12, 14-15, 27-28, 36, 41-42, 47-49, 55-56, 67-68, 72-79, 87, 96, and 102.

[✓] Install and solder 14-pin sockets in locations U2-5, 7, 17-20, 22, 24, 29, 31-33, 35, 43-46, 69-71, 88-92, 97, 100-101, and 105.

[✓] Install and solder 8-pin sockets in locations U6 and 86.

[✓] Install and solder a 33 pF disc ceramic capacitor at C116.

[✓] Install and solder 150 pF disc ceramic capacitors in locations C38 and 65

[✓] Install and solder 300 pF disc ceramic capacitors in locations C39 and 66

[ ] NOT NEEDED Install and solder 390 pF disc ceramic capacitors in locations C10-19 and C111-115.

[✓] Install and solder .01 uF disc ceramic capacitors in locations C1-2, 37, 54, and 59.

[✓] Install and solder 0.1 uF bypass capacitors in locations C3-9, 22-33, 36, 40-41, 43-53, 55-58, 60-64, and 67-110.

[✓] Paying careful attention to their polarity, install and solder 47 uF electrolytic capacitors in locations C20-21, 34-35, and 42.

[✓] Carefully check that the 47 uF capacitors are correctly installed.

[✓] Install and solder R38, a 10 Ohm 1/2 Watt resistor.

[✓] Install and solder R15, a 22 Ohm 1/4 Watt resistor.

✓ Install and solder R10, a 47 Ohm 1/4 Watt resistor.

✓ Install and solder R12, a 150 Ohm 1/4 Watt resistor.

[ ] Install and solder the following 220 Ohm, 1/4 Watt resistors: R6, 16, 24-25, 30-31, and 36-37.

[ ] Install and solder R14, a 680 Ohm 1/4 Watt resistor.

[ ] Install and solder the following 1.0K Ohm, 1/4 Watt resistors: R8-9, 11, 13, 18-19, ~~21~~, ~~23~~, ~~27~~, ~~29~~, ~~33~~, 35.

[ ] Install and solder R17, a 1.2K Ohm 1/4 Watt resistor.

[ ] Install and solder R3 and R4, 4.7K Ohm resistors.

[ ] Install and solder the following 10K Ohm, 1/4 Watt resistors: R5, 7, ~~20~~ ~~22~~, ~~26~~, ~~28~~, ~~32~~, and 34.

[ ] Install and solder R1 and R2, 33K Ohm 1/4 Watt resistors.

[ ] Install and solder RN1, RN2, and RN3.

[ ] Install and solder a 2N2222 or 2N2222A transistor at Q1.

[ ] Install and solder 2N2907 or 2N2907A transistors at Q2-Q8.

[ ] Install and solder 4148 diodes at CR1-11. Orient the diodes so that their banded ends are nearest the bars on the placement rectangles.

[ ] Install and solder Y1, an 8.000 MHz crystal.

[ ] Install and solder an 11.000 MHz crystal at Y2 if your CRT has a horizontal scan rate of 15.75 KHz, a 16.000 MHz crystal if your CRT has a horizontal scan rate of 18.6 KHz.

[ ] Install and solder 1x2 pin rows at JB14 and JB15.

[ ] Install and solder 1x3 pin rows at JB4, JB8, JB34, and JB35.

[ ] Install and solder a 1x4 pin row at JB10+JB11.

[ ] Install and solder 1x5 pin rows at JB7 and JB9.

[ ] Install and solder a 1x6 pin row at JB5. HARD WIRED

[ ] Install and solder 2x2 pin rows at JB13, JB16, JB19, JB22, JB25, JB28, and JB31.

[ ] Install and solder 2x3 pin rows at JB17, JB18, JB20, JB21, JB23, JB24, JB26, JB27, JB29, JB30, JB32, and JB33. Install a 2x3 pin row next to a 1x3 pin row in JB6. Solder both only when the pins of the resulting "3x3" pin row are four-square.

[ ] Install and solder a 2x5 pin row at JB12.

[✓] Install and solder a 2x6 pin row at JB2.

[✓] Install and solder 2x10 pin rows at J8-J11.

[✓] Install and solder 2x12 pin rows at JB1 and JB3.

[✓] Install and solder 2x13 pin rows at J2-J4

[✓] Install and solder a 2x17 pin row at J6.

[✓] Install and solder 2x25 pin rows at J5 and J7.

[✓] Install a four-position DIP switch at SW1.

[✓] Install a Star-Micronics QMB-06 beeper at DS1.

[✓] Install a ten-position terminal block at TB1.

[ ] Before installing any IC's in their sockets, apply power to the board and check that voltages are within five percent of their nominal values.

[ ] REMOVE POWER FROM THE BOARD BEFORE PROCEEDING!

[ ] Install 74LS00's in locations U29 and U31.

[ ] Install a 74LS02 in locations U25 and U71.

[ ] Install 74LS04's in locations U19, U43, U69, U91, and U101.

[ ] Install a 7406 in location U7.

[ ] Install a 7407 in location U44.

[ ] Install a 74LS08 in location U35.

[ ] Install a 74LS14 in location U17.

[ ] Install a 74LS30 in location U33.

[ ] Install 74LS32's in locations U46 and U97.

[ ] Install 7438's in locations U88, U89, and U90.

[ ] Install a 7445 in location U56.

[ ] Install 74LS74's in locations U18, U22, U26 U32, U70, U92, U100, and U105.

[ ] Install a 7486 or 74LS86 in location U24.

[ ] Install 74LS138's in locations U15, U27, and U55.

[] Install a 74LS139 in location U102.

[] Install a 74LS151 in location U12.

[] Install a 74157 in location U42.

[] Install 74LS157's in locations U47, U48, U49, U67, and U68.

[] Install a 74LS164 in location U45.

[] Install a 74LS169 in location U36.

[] Install a 74LS195 in location U28.

[] Install 74LS240's in locations U8 and U94.

[] Install 74LS244's in locations U9, U11, U38, U58, U63, U64, and U95.

[] Install 74LS245's in locations U40, U53, U54, U61, U65, and U66.

[] Install 74LS259's in locations U14, U41, and U96.

[] Install a 74LS273 in location U13.

[] Install 74LS73's in locations U1, U57, U59, U60, U93, U98, U99, U103, and U104.

[] Install a 74LS393 in location U20.

[] Install a 555 timer in location U86.

[] Install 1488's in locations U2 and U4.

[] Install 1489's or 1489A's in locations U3 and U5.

[] Install a 16-pin 220/330 Ohm DIP Resistor Network in location U87.

[] Install a Z80-A CPU in location U39.

[] Install a Z80-A DMA in location U62.

[] Install a Z80-A SIO/O in location U16.

[] Install Z80-A CTC's in locations U21 and U37.

[] Install a 6845S CRT controller in location U30.

[] Install an 8002 Video Attributes Controller in location U52.

[] Install a 1793, a 1797, or a Fujitsu MB8877 floppy disk controller in location U10.

[] Install a 9216B data separator in location U6.

[] Install the PAL16L8 in location U23.

[] Install the PAL10L8 in location U34.

[] Install the monitor EPROM in location U85.

[] Install eight 200 nS 4164 DRAM's in locations U72-U79.

[] Install two 200 nS 2Kx8 SRAM's in locations U50 and U51.

[] CAREFULLY CHECK THAT ALL IC'S ARE CORRECTLY INSTALLED IN THE PROPER SOCKETS.

[] Jumper that board as shown in the pages that follow.

[] Attach a parallel ASCII keyboard using J~~1~~ 2 and a CRT using JB~~5~~ 12.

[] Attach a reset switch to TB1.

[] Apply power to the board and type a <CR> at the keyboard. If all is well, a sign-on message will appear on the screen.

JUMPERING

Flopper-Disk Ready Signal

```
JB4
***   0 ┬ RDY Always True  --  Default for 5.25" Drives
      0 ┤
      : │
      0 ┴ RDY Asserted by Disk Drive  -- Default for 8" Drives
```

Jumper the middle pin to one of the other pins.

Video Output

```
                 V     H     V
                 i     o     e
                 d     r     r
                 e     i     t
                 o     z

                 0     0     0        If the middle row is jumpered to the
                                :      top row, the signal will be inverted.
                                :
          JB6    0     0     0
          ***    :     :
                 :     :              If the mniddle row is jumpered to the
                 0     0     0        bottom row, the signal is UNinverted.

                 S     S     S
                 i     y     y
                 g     n     c
                 n     c
                 a
                 l
```

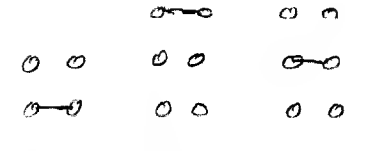
Character Dot-Matrix

JB12

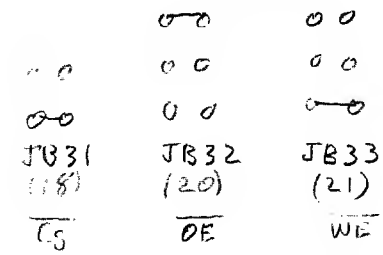
			JB13
GROUND	0	0	
	0	0	
	0	0	****
SIDE	0	0	0--0
	0	0	0--0

Install jumpers as shown for 7x9 characters. Omit both jumpers for 5x7 characters.

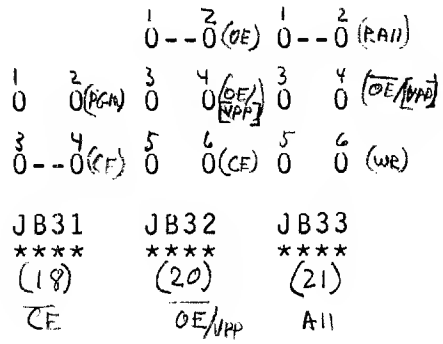
2716 STRAPPING



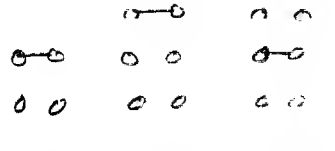
2K RAM



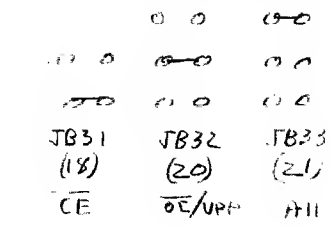
2732(A) Strapping



2716 PROGRAM

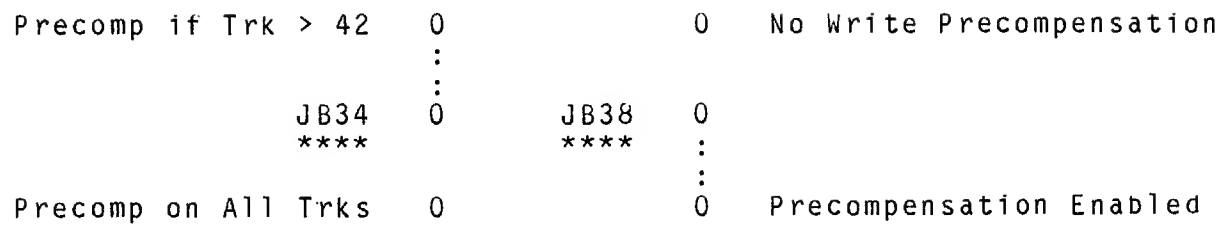


2732 PROGRAM



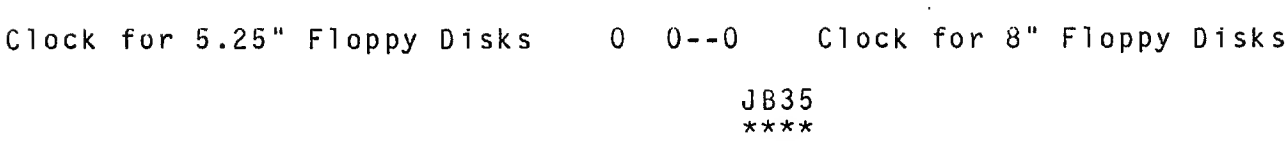
  SUBJECT TO REVISION

Write Precompensation

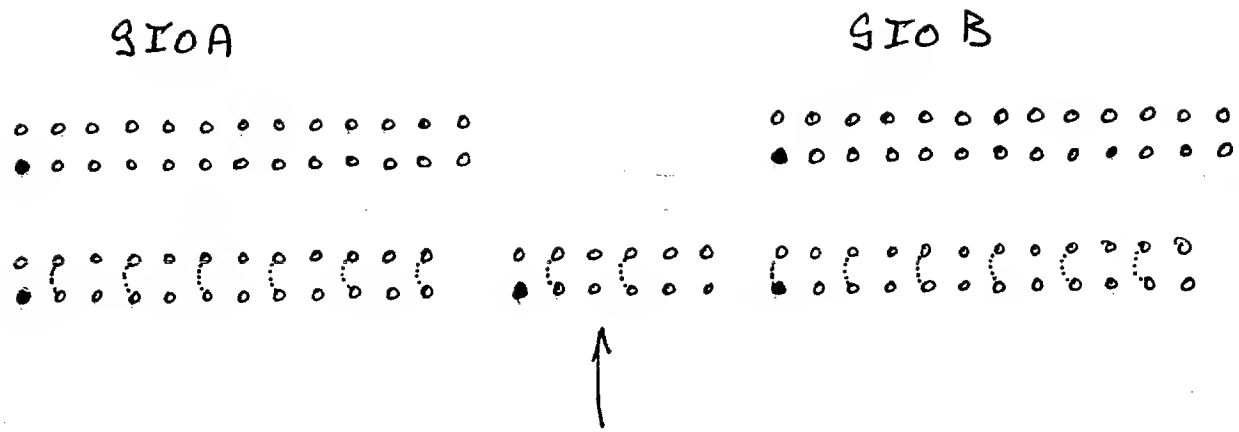


Jumper each of the middle pins to one of the other pins.

Data-Separator Clock



Jumper the middle pin to one of the other pins



SIO A SHOWN STRAPPED FOR COMMUNICATION WITH A MODEM

SIO B SHOWN STRAPPED FOR COMMUNICATION WITH A TERMINAL

Taylor ELECTRIC COMPANY

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BETTER BOARD UPDATE

08/20/82

This update lists several modifications recommended by Cal-Tex as well as some hints on bringing up a Better Board after construction. Some preliminary documentation of the Better Board monitor is also included.

JUMPERS: The label for the write precompensation enable/disable jumper field in the Assembly Manual is incorrect. It should be JB8 instead of JB38. This jumper is listed on Page 18 of the manual.

If you wish to use the serial ports you must add jumpers to JB1 (for Serial Port A) and/or JB3 (for Serial Port B) and to JB2 (baud rate clock). The jumpers on JB1 and JB3 are identical and determine whether the associated port is configured as a terminal (Data Terminal Equipment) or a modem (Data Communications Equipment):

Terminal (DTE)	Modem (DCE)
3-4	1-2
7-8	5-6
11-12	9-10
15-16	13-14
19-20	17-18
23-24	21-22

To connect a serial terminal to the Better Board, install the "Modem" jumpers. To connect the Better Board to a modem, install the "Terminal" jumpers.

JB2 is used to select the source for the Serial I/O chip's clock. For normal operation with the Better Board's monitor jumper pins 3-4 and 7-8. This selects the output of one of the Clock Timer Chips (CTC U-21, section 1) as the source for the SIO chip's clock.

All other jumpers should be set up as shown in the Assembly Manual.

SWITCH SETTINGS: The four position DIP switch (SW1) is used to select

various software options. The normal configuration is with sections 1 through 3 ON (to the right or away from power connector) and section 4 OFF.

Section 3 selects the disk drive size and should be turned OFF if 5" floppy drives will be used with the board. If 5" drives are to be used, it is also necessary to change the jumpers on JB4 (Page 16), JB38 (Page 18) and JB35 (Page 18). The default is for 8" drives.

Section 4 determines whether the CRT controller will be programmed for 5x7 or 7x9 characters. This switch should be turned ON for 5x7 characters. If this switch is turned on you must also remove the jumpers on JB13, change U5Q to a CRT8002B-003, and change Y2 to an 11 MHz crystal. These changes are necessary if you wish to use the Better Board with a CRT utilizing a 15.75 KHz horizontal scan rate. The default configuration (7x9 characters) requires a CRT with an 18.6 KHz horizontal scan rate.

PALS: The Better Board uses two PALS. Originally, one was a 10L8 (U34) and the other was a 16L8 (U23). Cal-Tex discovered a programming error in an early lot of the 10L8's and replaced them with 16L8's. If you find that there are two 16L8's in your kit, the one stamped with the lot code "BB2U34R1" is to be used in place of the 10L8 at U34. WARNING: The lot code on some of the PALS is stamped upside down. Be sure to use the molded dot on the device case to locate pin 1—don't be fooled by the lot code.

BRINGING UP BB: The monitor EPROM supplied with the Better Board does a CRC check of itself and a read/write check of the RAM into which the monitor is copied when power is applied to the board. If both tests are passed, the on-board beeper will sound briefly. The EPROM then proceeds to initialize the board's programmable I/O devices. When this is done the program loops through a check of the parallel keyboard and each of the two serial ports. When a carriage return character is entered through one of these ports, the software identifies the port and designates it as the console device. In the case of the serial ports, the system detects the baud rate at which the carriage return was sent and switches to that speed for subsequent communications. In the case of the parallel keyboard port, the system detects the polarity of the keyboard strobe and stores it for future use.

The first step in bringing up a new board is to determine whether the beeper sounds approximately 2 seconds after power is applied. If it does, it means that the EPROM and RAM can be accessed and are functional. Any subsequent problems will probably be related to the I/O devices. If the beeper fails to sound, it means that the processor, memory or EPROM are not functioning properly

Once the board passes the beeper test you should attempt to sign on. If you are using the parallel keyboard port and built-in CRT driver, simply press the carriage return key on the keyboard. The monitor's sign-on message should appear on the CRT. Alternatively, you may connect a

serial terminal to one of the board's serial ports. Make sure that the appropriate jumpers have been installed (see above). Pressing the carriage return key should cause the sign-on message to appear on the serial terminal.

DISPLAY CHANGE: (This change applies only to systems using the built-in CRT driver with the standard 7x9 dot matrix). Some CRT's will give a more stable display if the CRT controller chip is programmed for different horizontal and vertical synch timing than that provided by the monitor EPROM. You can change the programming from the monitor with the following command sequence:

```
ODC,2
ODD,5F
ODC,0
ODD,6F
ODC,7
ODD,18
```

MONITOR FUNCTIONS: The Better Board monitor is very similar to that provided with the Big Board. The documentation currently available from Cal-Tex does not provide any description of the monitor's functions. We have compiled a list of monitor functions by comparing the Big Board's documentation with the Better Board's monitor source code. A copy is attached for your convenience.

CRT DRIVER CODES: The built-in CRT driver responds to the same control codes as the Big Board with the exception that erase to end of screen (EOS) has been changed from a control-W to a control-Q. The control codes are:

^G	Bell
^H	Cursor Left (Backspace)
^I	Horizontal Tab
^J	Cursor Down (Linefeed)
^K	Cursor Up
^L	Cursor Right
^M	Carriage Return
^Q	Clear to End of Screen
^X	Clear to End of Line
^Z	Clear Screen and Home
^[	Escape Sequence Lead-in (see below)
^^	Cursor Home
^_	Display Control Character

The Better Board uses the same escape sequence as the Big Board for cursor control. In addition, it supports a number of new functions. The escape sequences are:

ESC = row col	Cursor Addressing
ESC Q	Insert Character
ESC W	Delete Character
ESC E	Insert Line
ESC R	Delete Line
ESC *	Clear Screen and Home
ESC :	Clear Screen and Home
ESC T	Clear to End of Line
ESC t	Clear to End of Line
ESC Y	Clear to End of Screen
ESC y	Clear to End of Screen
ESC G attr	Set Attribute
ESC M mode	Set Graphics Mode
ESC . byte	Set Parameter Byte

The row and column numbers in the cursor addressing sequence are formed by taking the row number (0 to 23) or column number (0 to 79) and adding 20H (i.e., an ASCII space character) to it.

The attribute character takes one of the following ASCII values:

0	Normal ASCII
1	Underlined ASCII
2	Blinking ASCII
3	Underlined, Blinking ASCII
4	Reverse Video ASCII
5	Reverse Video, Underlined ASCII
6	Reverse Video, Blinking ASCII
7	Reverse Video, Underlined, Blinking ASCII
8	Normal Graphics
9	Underlined Graphics
A	Blinking Graphics
B	Underlined, Blinking Graphics
C	Reverse Video Graphics
D	Reverse Video, Underlined Graphics
E	Reverse Video, Blinking Graphics
F	Reverse Video, Underlined, Blinking Graphics

When a value from 8 through F is specified for the attribute, the display switches to one of the graphics modes. The modes are:

0	Block Graphics Mode
1	Bar Graphics Mode #1
2	Bar Graphics Mode #2
3	ASCII Character Set mode

The allowed values for the parameter byte are the following ASCII characters:

0	No auto-newline, normal scroll, no clock display
1	Auto-newline, normal scroll, no clock display
2	No auto-newline, no scroll, no clock display
3	Auto-newline, no scroll, no clock display
4	No auto-newline, normal scroll, clock is displayed

5 Auto-newline, normal scroll, clock is displayed
6 No auto-newline, no scroll, clock is displayed
7 Auto-newline, no scroll, clock is displayed
(Clock Display is not implemented in current monitor)

SOFTWARE COMPATIBILITY: The Better Board uses the same monitor entry points that were used by the Big Board. This means that software which runs on the Big Board will also run on the Better Board provided that all hardware access is made via the system monitor entry points. This includes the Big Board CP/M which will run (although only in single density) without modification on the Better Board.

* - * - *

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BETTER BOARD MONITOR COMMANDS

08/20/82

Command	Format
d(ump)	D <start>,<end>
m(emory)	M <address>
t(est)	T <start>,<end>
f(ill)	F <start>,<end>
c(opy)	C <source start>,<source end>,<dest start>
v(erify)	V <source start>,<source end>,<dest start>
x(change)	X <bank number>
g(oto)	G <address>
r(ead)	R <unit>,<track>,<sector>
b(oot)	B
i(nput)	I <port>
o(output)	O <port>,<data>

1) DUMP COMMAND: The dump command outputs a tabular display of the contents of memory in hexadecimal and ASCII representation. Each display line has the following format:

AAAA DD DD DD DD DD DD DD ... DD DD CCCCCCCCCCCCCCCC

where AAAA is the starting memory address of the line in hexadecimal, the DD's are the hex values of the 16 bytes of data starting at location AAAA, and the C's are the ASCII characters equivalent to each data byte. Bytes less than 20 hex are replaced in the ASCII portion of the dump by periods.

The dump command accepts zero, one or two address parameters. If two addresses are specified, the block of memory between those two locations will be displayed. Entering only one address will display 256 bytes of memory

starting at the specified location. Typing 'D' with no parameters will cause the routine to display the 256 byte block of memory starting at the last address displayed by the dump command.

2) MEMORY COMMAND: The memory examine/change command allows the contents of individual memory locations to be read from and written into using the monitor. This command accepts one parameter representing the memory address at which to begin examining data. The display format is as follows;

AAAA DD _

where AAAA is the current memory address and DD is the hexadecimal value of the data in that location. After displaying the contents of a memory location, the routine waits for one of the following items to be input from the console:

- Typing a carriage return will cause the routine to display the data at the next memory location, with no modification of the contents.
- Typing a minus sign will have a similar effect, except the address is decremented instead of incremented.
- Typing a two digit hexadecimal number will cause that number to be stored at the displayed address. The new data is stored as soon as the second digit is entered, with no terminating character required.
- Typing any character other than carriage return, a minus sign or a hexadecimal digit will cause the command to terminate.

3) TEST COMMAND: The command allows the user to test memory for errors caused by defective memory chips, solder bridges and various other problems. Any portion of memory may be tested except the area reserved for the monitor (F000 to FFFF hex). Two parameters are required from the user; the starting address and ending address of the memory block to be tested. Only the high order 8 bits of the addresses entered are actually used however, due to a characteristic of the test algorithm being employed. If no errors occur, the test routine will output a plus sign every time a test pass is done. A total of 256 plus signs must be output for all possible test patterns to have been tried. When errors are detected an error line will be output in the following format:

AAAA DD should =XX

where AAAA is the address of a location that fails to test, DD is the data read back from that location, and XX is the test pattern that was written there.

4) FILL COMMAND: The fill command allows blocks of memory to be filled with a fixed data constant. Three parameters are required in the command line; a starting memory address, an ending address and a fill constant. Each location the specified block of memory has the constant written into it and then read back again to check for memory errors. An error line like the one described for the 'T' command is printed for any locations that fail to verify.

5) COPY COMMAND: The copy command allows blocks of data to be moved in memory. Three parameters are required in the command line; a starting memory address, an ending address, and a destination address. The contents of the block of memory bounded by the first two addresses is copied to the block starting at the third address. As with the fill command, a test is made to verify that each byte of the destination block, when read back, is the same as the corresponding byte in the source block.

6) VERIFY COMMAND: The verify command allows the contents of two blocks of memory to be compared with each other byte by byte. This command has the same syntax as the copy command. Each byte in the source block is compared with the corresponding byte in the destination block. Any locations that are not the same will cause a memory error message line to be displayed. If both blocks are identical nothing is output and control simply returns to the monitor.

7) EXCHANGE MEMORY BANKS COMMAND: This command allows switching memory banks. If used with no parameter, the current memory bank configuration will be displayed as a number from 00 to 03. This number represents the two bit binary code which controls the Better Board's memory banks. When Bit 0 is off the monitor EPROM and the CRT static RAM are addressed as the lower 32K. When Bit 0 is on, the lower 32K addresses the same type of RAM as is selected for the upper 32K. Bit 1 determines whether the upper 32K addresses on-board dynamic RAM (Bit 1 off) or off-board RAM via the STD buss (Bit 1 on). Thus:

```
00 :: 0-32K = Monitor EPROM  CRT RAM, 32-64K = BB DRAM
01 :: 0-64K = BB DRAM
02 :: 0-32K = Monitor EPROM  CRT RAM, 32-64K = STD RAM
03 :: 0-64K = STD RAM
```

If this command is used with a parameter, the appropriate

memory bank(s) are selected in accordance with the table above. The RAM resident portion of the monitor is copied to the new bank if necessary. If the new bank is not present or an error is detected as the monitor is being copied, the error message "E:R AT AAAA" is displayed and the previously selected configuration is restored.

Certain of the monitor's functions are always executed out of the EPROM. If a configuration is selected which switches out the EPROM, it is automatically switched back in whenever necessary. This activity is invisible to the user. If you are using the built-in CRT driver you can examine the CRT's memory map by selecting configuration 00 or 02. The screen buffer begins at 6000H and the attribute table begins at 7000H.

8) GOTO COMMAND: The goto command allows control of the CPU to be passed to another program by the monitor. This command requires a single parameter from the user representing the address at which to begin execution. The monitor actually passes control to the specified location by executing a CALL instruction. This makes it possible for the external routine to return to the monitor by doing a RET, assuming it does not re-load the stack pointer to lose the return address to the monitor.

9) READ COMMAND: The read command allows individual disk sectors to be read into memory and displayed on the console. Three parameters are required; a drive unit number (range 0 to 3), a track number (range 0 to 4C) and a sector number (range 1 to 1A). The command routine performs a drive select, track seek and a sector read sequence using the supplied parameters. If no errors occur, the contents of the input buffer will be dumped out in the 'D' command format. In the event of a disk error, a diagnostic message will be printed in the following format:

disk error XX SD UAA TBB SCC

Where XX represents the disk controller error status code, SD indicates single density mode (replaced by DD when in double density mode), AA is the unit number, BB is the track number, and CC is the sector number. The error code is composed of the eight bits of status information returned by the disk controller represented as a hexadecimal number.

10) BOOT COMMAND: The boot command is used to load and begin execution of a one sector long bootstrap loader from the first sector on drive unit zero. The most common use of this command will be to boot up the CP/M* disk operating system, although it is not necessarily restricted to this purpose only.

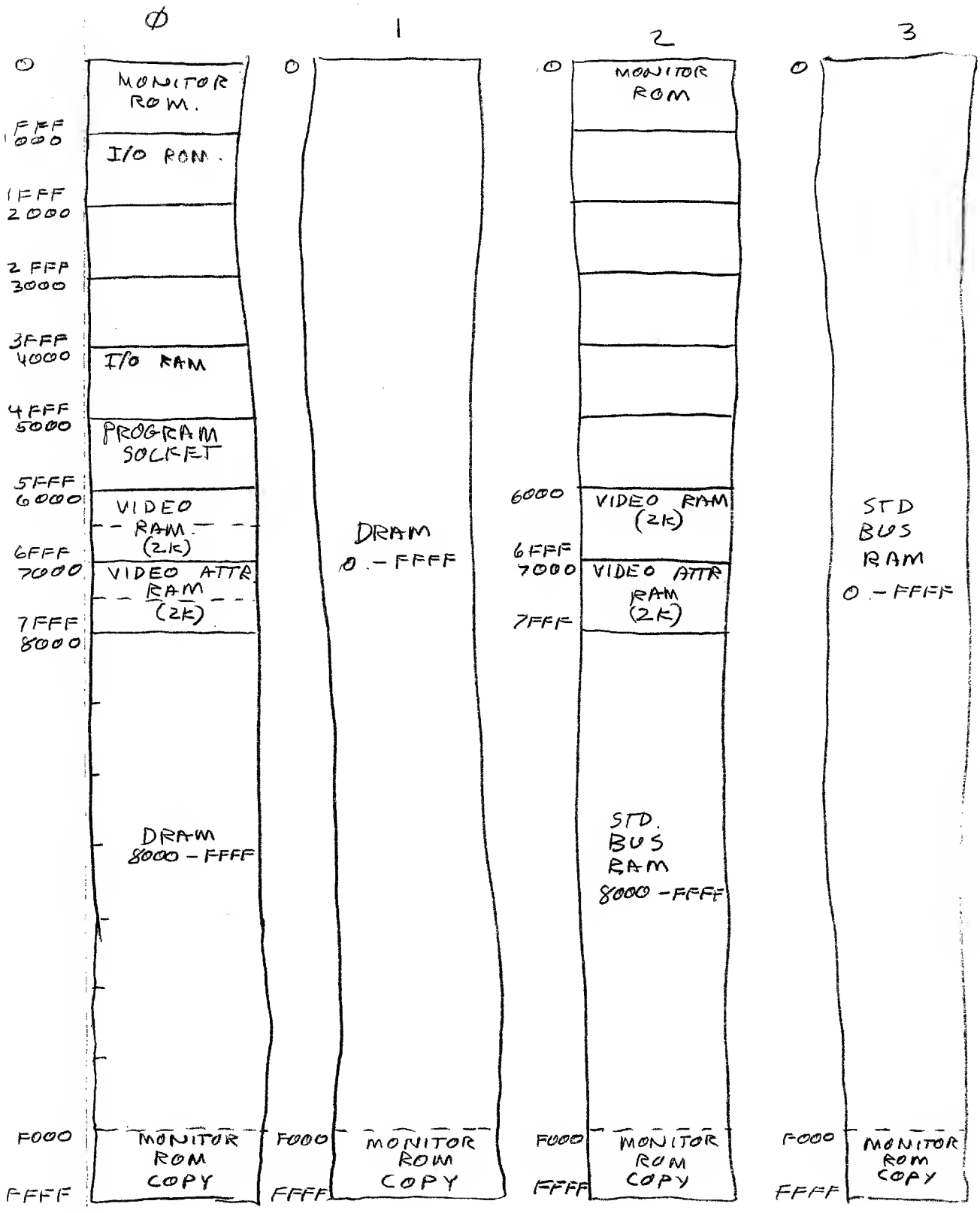
The boot works by reading the contents of track 0, sector 1 into memory at location 80 hex and then jumping to that address to start execution of the code just read in. Normally the routine on sector 1 will be a small loader that in turn reads in a larger program such as the operating system. This two level bootstrap process makes the boot command more application independent. The only requirements are that the first sector of the boot diskette be reserved for a loader and that the bottom 256 bytes of memory are not written over by the program being loaded.

*CP/M is a registered trademark of Digital Research

11) INPUT COMMAND: This command allows the contents of input ports to be read using the monitor. It operates very much like the memory examine command, except that input ports are being examined instead of memory locations. A single parameter representing a port number is expected in the command line. the contents of adjacent ports can then be examined by typing carriage return or a minus sign as in the 'M' command. Typing any other key will cause the routine to terminate.

12) OUTPUT COMMAND: The output command is provided to allow output ports to be written to using the monitor. Two parameters are expected in the command line; a port number and a data byte to be output to that port. Both parameters should be between 0 and FF hex. After outputting the specified data to the port, this routine simply returns to the monitor instead of stepping to the next location like the input command. This makes it possible to use the output command to initialize Z-80 peripheral devices like the SIO, PIO and CTC.

* - * - *


BANK
Ø
1
2
3
0
MONITOR ROM.
FFF 1000
I/O ROM.
1FFF 2000
2FFF 3000
3FFF 4000
I/O RAM
4FFF 5000
PROGRAM SOCKET
5FFF 6000
VIDEO RAM (2K)
6FFF 7000
VIDEO ATTR RAM (2K)
7FFF 8000
DRAM 8000 - FFFF
F000
MONITOR ROM COPY
FFFF
DRAM 0 - FFFF
MONITOR ROM
6000
VIDEO RAM (2K)
7000
VIDEO ATTR RAM (2K)
7FFF
STD. BUS RAM 8000 - FFFF
STD BUS RAM 0 - FFFF

J2
KEYBOARD

PIN		
1	KD Ø	
2	GND	
3	KD 1	
4	GND	
5	KD 2	
6	GND	
7	KD 3	
8	GND	
9	KD 4	
10	GND	
11	KD 5	
12	GND	
13	KD 6	
14	GND	
15	KD 7	
16	GND	
17	KBDSTB	(+STROBE)
18	GND.	
19	+12V	
20	+12V	
21	?	
22	−12V	
23	−12V	
24	?	
25	+5V	
26	+5V.	

J3 & J4
SERIAL I/O

PIN	
1	CH GND
2	TXD
3	RxD
4	RTS
5	CTS
6	DSR (+12V THRU 4700Ω)
7	SIG. GND
8	DCD
9	
10	
11	
12	
13	
14	
15	TX CLK (J3 ONLY)
16	
17	RX CLK (J3 ONLY)
18	
19	
20	DTR.
21	
22	
23	
24	
25	
26	

J5 8" FLOPPY

PIN	
1-.49	GND
2	LOW CURRENT
4	
6	
8	
10	
12	
14	SIDE SELECT
16	
18	HEAD LOAD
20	INDEX
22	READY
24	
26	SELECT Ø
28	SELECT 1
30	SELECT 2
32	SELECT 3
34	DIRECTION CONTROL
36	STEP
38	WRITE DATA
40	WRITE GATE
42	TRACK ØØ
44	WRITE PROTECT
46	READ DATA
48	
50	

J6 5" FLOPPY I/O

PIN	
1..33	GND
2	
4	
6	
8	INDEX
10	DS Ø
12	DS 1
14	DS 2
16	MOTOR ON
18	DIRECTION CONTROL
20	STEP
22	WRITE DATA
24	WRITE GATE
26	TRACK ØØ
28	WRITE PROTECT
30	READ DATA
32	SIDE SELECT
34	

J7 SASI I/O.

PIN.	
1 .. 49	GND
2	DATA Ø
4	DATA 1
6	DATA 2
8	DATA 3
10	DATA 4
12	DATA 5
14	DATA 6
16	DATA 7
18	
20	
22	
24	
26	
28	
30	
32	
34	
36	BUSY
38	ACK
40	RESET
42	MESSAGE
44	SELECT
46	COMMAND/DATA
48	REQUEST
50	I/O

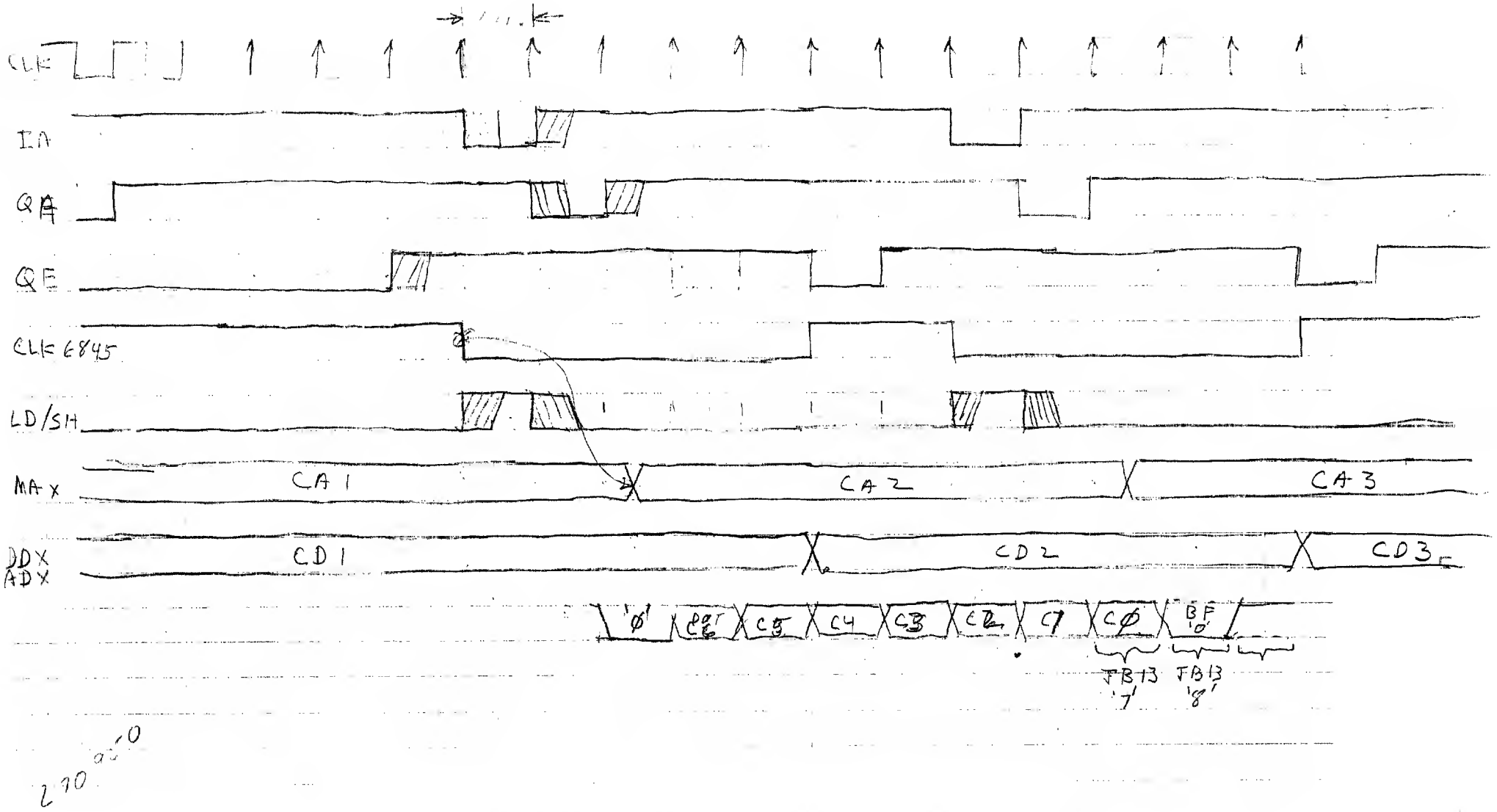
J8 -- J11 PARALLEL I/O

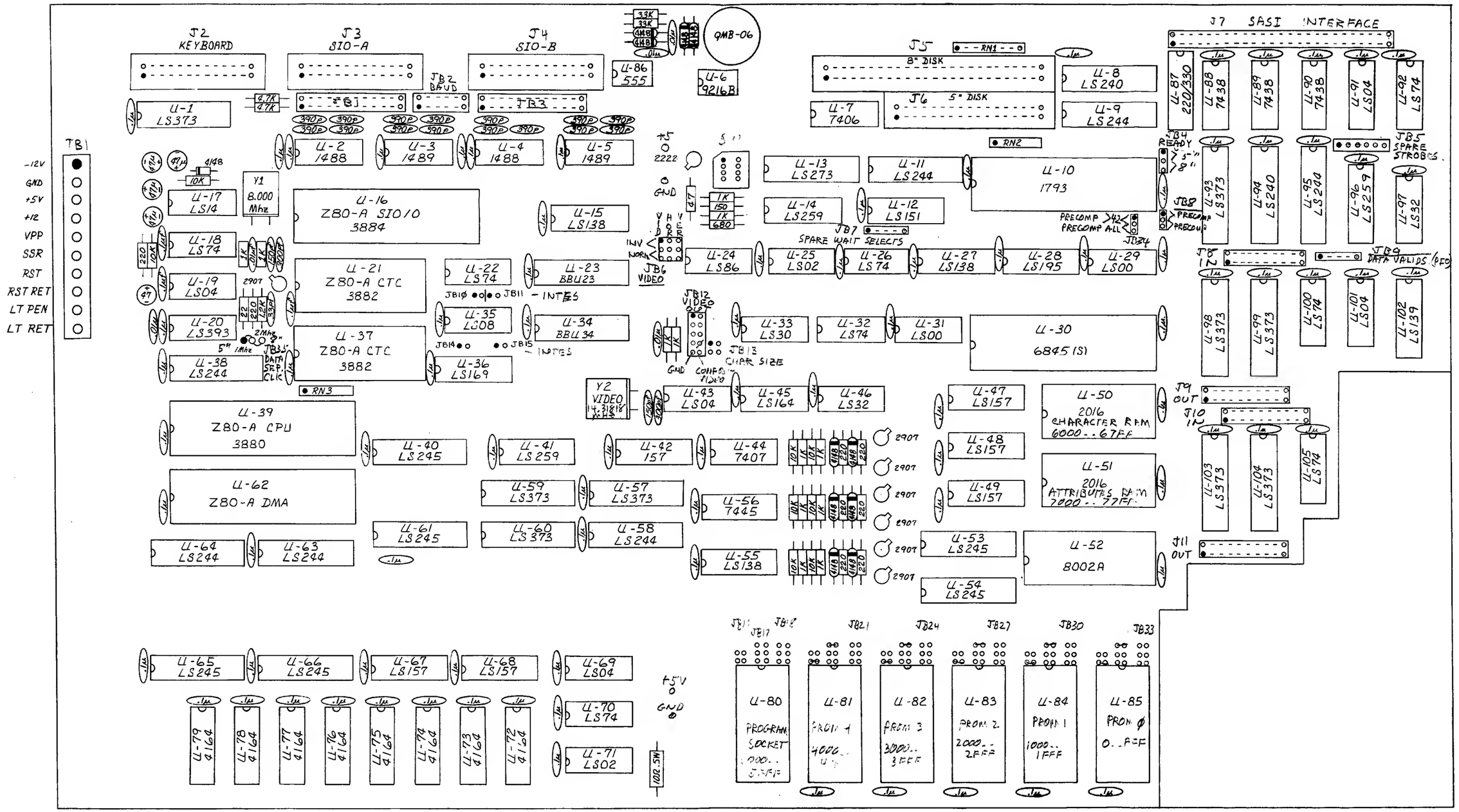
PIN	J8	J9	J10	J11
1	I3Ø	O3Ø	I2Ø	O2Ø
2	GND			
3	I31	O31	I21	O21
4	GND			
5	I32	O32	I22	O22
6	GND			
7	I33	O33	I23	O23
8	GND			
9	I34	O34	I24	O24
10	GND			
11	I35	O35	I25	O25
12	GND			
13	I36	O36	I26	O26
14	GND			
15	I37	O37	I27	O27
16	GND			
17	IDAV1	ODAV1	IDAV2	ODAV2
18	GND			
19	GIVE1	$\overline{\text{TAKE1}}$	GIVE2	$\overline{\text{TAKE2}}$
20	GND	$\overline{\text{OE1}}$		$\overline{\text{OE2}}$

ALL UNSPECIFIED PINS ARE GROUNDS.

J12 VIDEO

PIN	
1	GND
2	SEPARATE VIDEO
3	GND
4	H. SYNC.
5	GND
6	V. SYNC.
7	GND.
8	N/C.
9	GND
10	COMPOSIT VIDEO


CLK
IN
QA
QE
CLK 6845
LD/SH
MAX
CA1
CA2
CA3
DDX
ADX
CD1
CD2
CD3
'0'
C6
C5
C4
C3
C2
C1
C0
BF
'0'
FB13
'7'
FB13
'8'



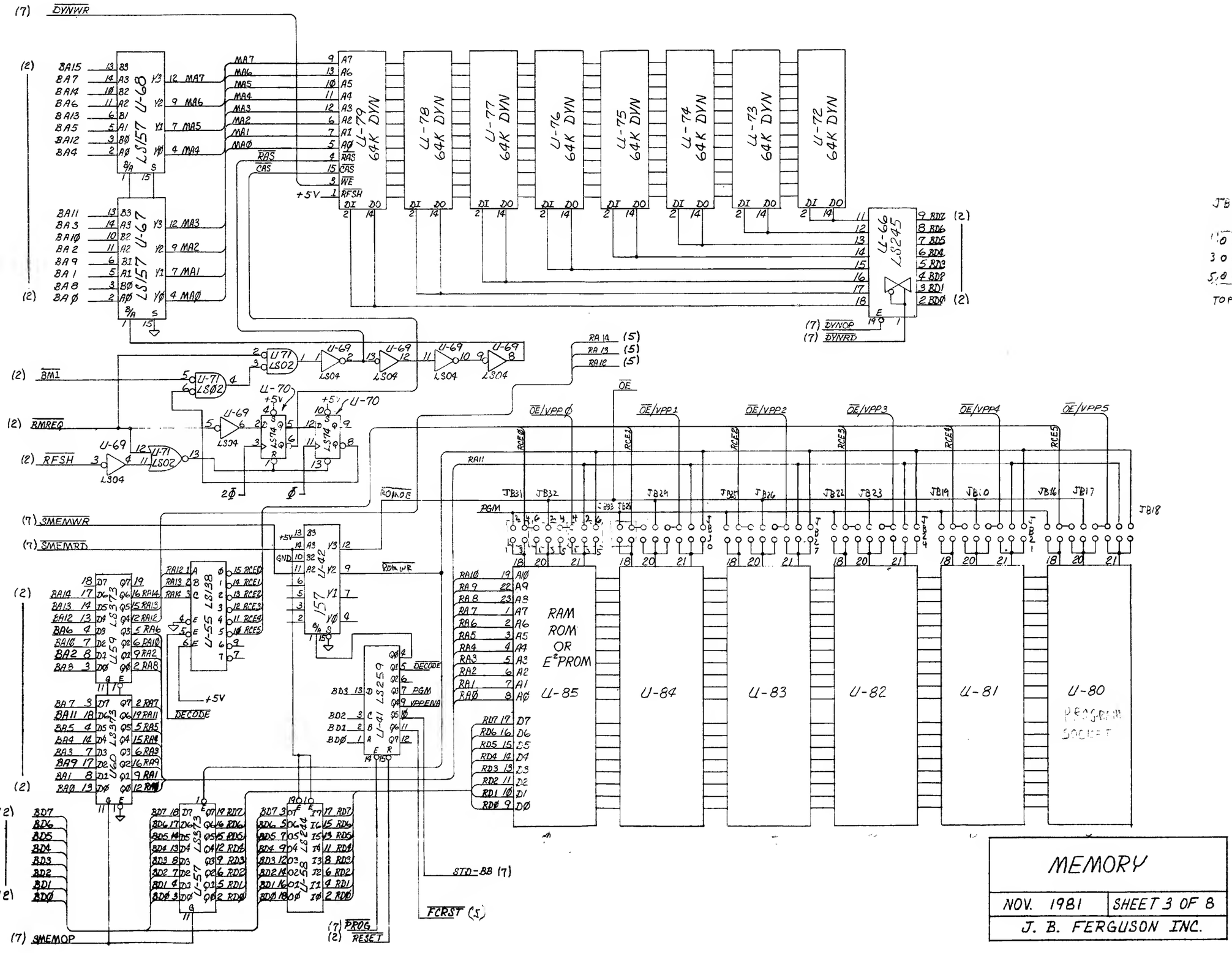
COMPONENT LAYOUT	
JUNE 1983	SHEET 1 OF 8
J. B. FERGUSON INC.	

+5V
10K R5
1N4148 CR5
.47µf C21
U-17 LS14
U-17 LS14
+5V
+5V
10K R7
220 R6
.01µf C54
.47µf C42
U-17 LS14
LS74 U-18
LS74 U-18
U-17 LS14
U-17 LS14
CK 1/2 74LS393 U-20
R QA QB QC QD
NC NC NC
BM1 13
12 LS04 U-19
BM1 (2,7)
2 U-19 LS04
RESET (3
R9 1K
R8 1K
C37 .01
5 6 1 LS04 U-19
CK 1/2 74LS393 U-20
R Q1 Q2 Q3 Q4
.5 Mhz
1 Mhz
2 Mhz
+5V
22 R15
C38 150 pf
9 8 LS04 U-19
C39 300pf
8.000 Mhz Y-1
1.2K R17
220 R16
33pf C116
2N2907 Q2
3 4 U-19
2Φ
Φ
+5V .1 GND
11 VCC 29 VSS
6 Φ
+5V .1 GND
11 VCC 30 VSS
7 Φ
Z80-A CPU U-39
Z80-A DMA U-62
A15 5
A14 4
A13 3
A12 2
A11 1
A10 40
A9 39
A8 38
A7 37
A6 36
A5 35
A4 34
A3 33
A2 32
A1 31
A0 30
D7 13
D6 10
D5 9
D4 7
D3 8
D2 12
D1 15
D0 14
M1 27
MREQ 19
IORQ 20
RD 21
WR 22
RFSH 28
RDY 25 RDY
INT 37 INT
BUSRQ 25 BUSRQ
BUSAK 23 BAI
BAO 13
IEI +5V 38
IEO 36 DMAIEO (6)
RFSH
CE (7) DMACE 16
+5V 10K RN3-5 MDBUSRQ
A15 17
A14 18
A13 19
A12 20
A11 21
A10 22
A9 23
A8 24
A7 39
A6 40
A5 1
A4 2
A3 3
A2 4
A1 5
A0 6
D7 27
D6 28
D5 29
D4 31
D3 32
D2 33
D1 34
D0 35
M1 26
MREQ 12
IORQ 10
RD 9
WR 8
LS245 U-40
IOD7 11
IOD6 12
IOD5 13
IOD4 14
IOD3 15
IOD2 16
IOD1 17
IOD0 18
1 E 19
(7) IOBUFD
9 BD7 (2)
8 BD6
7 BD5
6 BD4
5 BD3
4 BD2
3 BD1
2 BD0
LS244 U-63
A15 6
A14 13
A13 8
A12 11
A11 17
A10 2
A9 4
A8 15
1 E E 19
14 BA15 (3,4)
7 BA14
12 BA13
9 BA12
3 BA11
18 BA10
16 BA9
5 BA8
LS244 U-64
A7 8
A6 11
A5 2
A4 17
A3 4
A2 15
A1 6
A0 13
1 E E 19
12 BA7 (3-8)
9 BA6
18 BA5
3 BA4
16 BA3
5 BA2
14 BA1
7 BA0
LS245 U-61
D7 9
D6 8
D5 7
D4 6
D3 5
D2 4
D1 3
D0 2
1 E 19
(7) CPURD
(2) DMADIS
11 BD7 (2-4,7)
12 BD6
13 BD5
14 BD4
15 BD3
16 BD2
17 BD1
18 BD0
LS244 U-38
M1 4
MREQ 15
IORQ 11
RD 13
WR 8
6
1 E E 19
16 BM1 (7)
5 BMREQ (7)
9 BIORQ (2,7)
7 BRD (7)
12 BWR (7)
14 BRFSH (7)
RN3-6 10K +5V
(2) DMAIEO
(7) INTAK
U25 '02
(7) DMACE
(2) BIORQ
U25 '02
U25 '02
DMADIS (2)
(2) BM1
(2) Φ
+5 +5V
U26 '74
U26 '74
+5V
U46 '32
(7) SMEMDP
NC. 26 RESET
18 HALT
+5V 10K RN3-3 24 WAIT
(7) NMIRQ +5V 10K RN3-4 17 NMI
(6,7) INT +5V 10K RN3-2 16 INT

C. P. U.

JUNE '83 | SHEET 2 OF 8

J. B. FERGUSON INC.



MEMORY

NOV. 1981	SHEET 3 OF 8
J. B. FERGUSON INC.	

R18 1K R19 1K .01 U-43 LS04 C65 150pf U-43 LS04 300pf C66 Y2

U-45 74LS164 LS74 U-32 JB 13 LS30 U-33 U43 LS04 +5V

U-30 6845(S) VCC RES E R/W CLK CS RS MA13 MA12 MA11 MA10 MA9 MA8 MA7 MA6 MA5 MA4 MA3 MA2 MA1 MA0 RA4 RA3 RA2 RA1 RA0 VSYNC HSYNC DISPTMG CUDISP VSS LPSTB LPEN TBI-24 IOD7 IOD6 IOD5 IOD4 IOD3 IOD2 IOD1 IOD0 BRD BWR 6845CE BA0

U-47 LS157 U-48 LS157 U-49 LS157 MA0 MA1 MA2 MA3 MA4 MA5 MA6 MA7 MA8 MA9 MA10 BA0 BA1 BA2 BA3 BA4 BA5 BA6 BA7 BA8 BA9 SA0 SA1 SA2 SA3 SA4 SA5 SA6 SA7 SA8 SA9 SA10

U-50 2016 CHARACTER RAM

U-51 2016 ATTRIBUTES RAM

BUSS A BUSS B RA BUSS DISPTMG U-32 LS174 NC U-31 -00 +5V

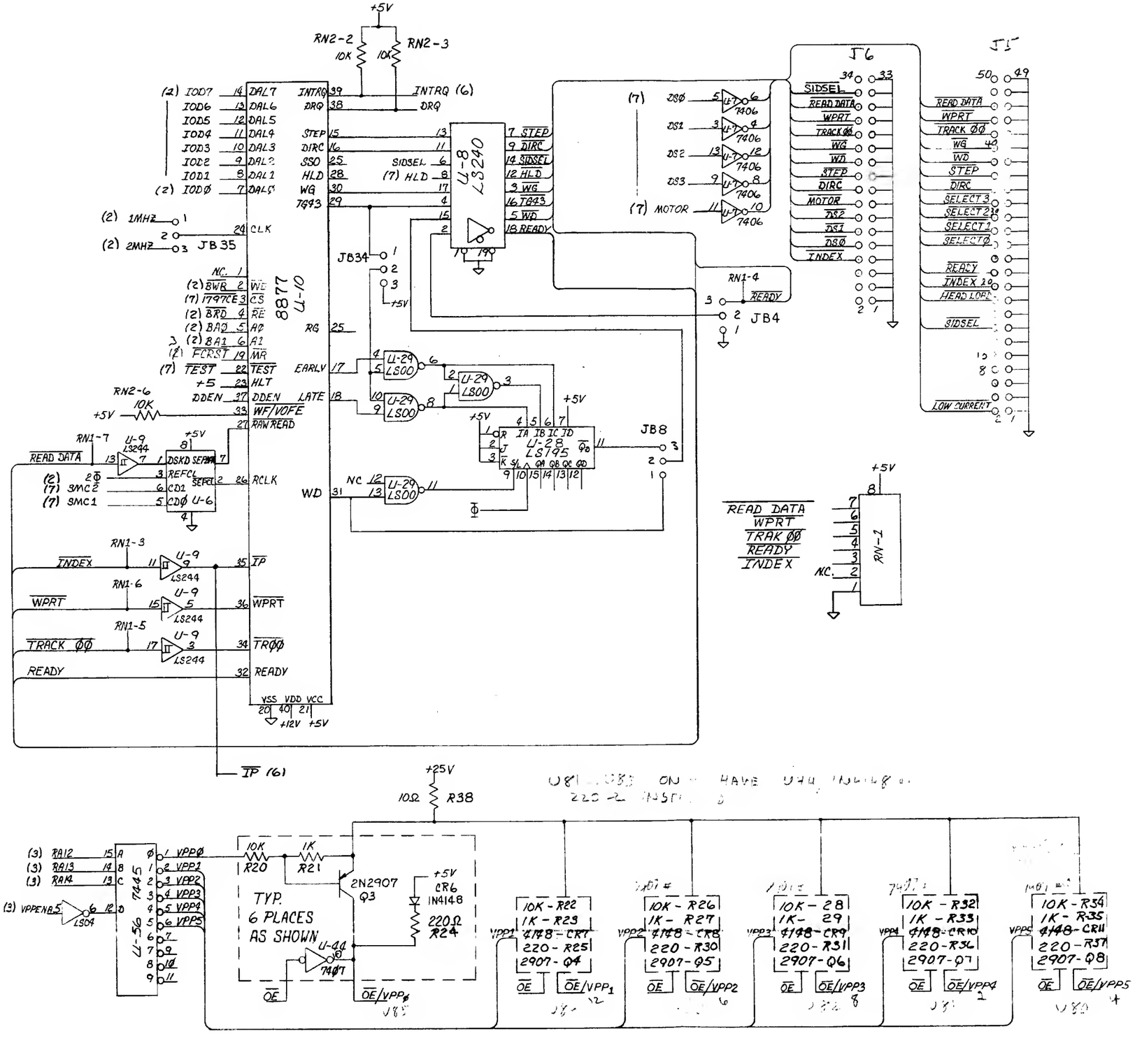
U-52 8002A VSYNC CURSOR DD7 DD6 DD5 DD4 DD3 DD2 DD1 DD0 RETBL BLINK CHABL REVID U/YDLN STKRU MI M0 VDC LD/SH ATTBE RA3 RA2 RA1 RA0 R3 R2 R1 R0

U-54 LS245 U-53 LS245 BD7 BD6 BD5 BD4 BD3 BD2 BD1 BD0 BRD ATTCE CHARCE

HSYNC VSYNC U-24 LS86 U43 R14 680Ω R11 1K R13 1K 2N2222 R10 49Ω 150Ω R12 VIDEO J12-10 J12-9 SEPARATE VIDEO J12-2 J12-1 P/O JB6 HSYNC 12 BHSYNC J12-4 J12-3 VSYNC 2 BVSYNC J12-6 J12-5

C R T

JUNE 1983	SHEET 4 OF 8
J. B. FERGUSON INC.	



FLOPPY DISK CONTROL

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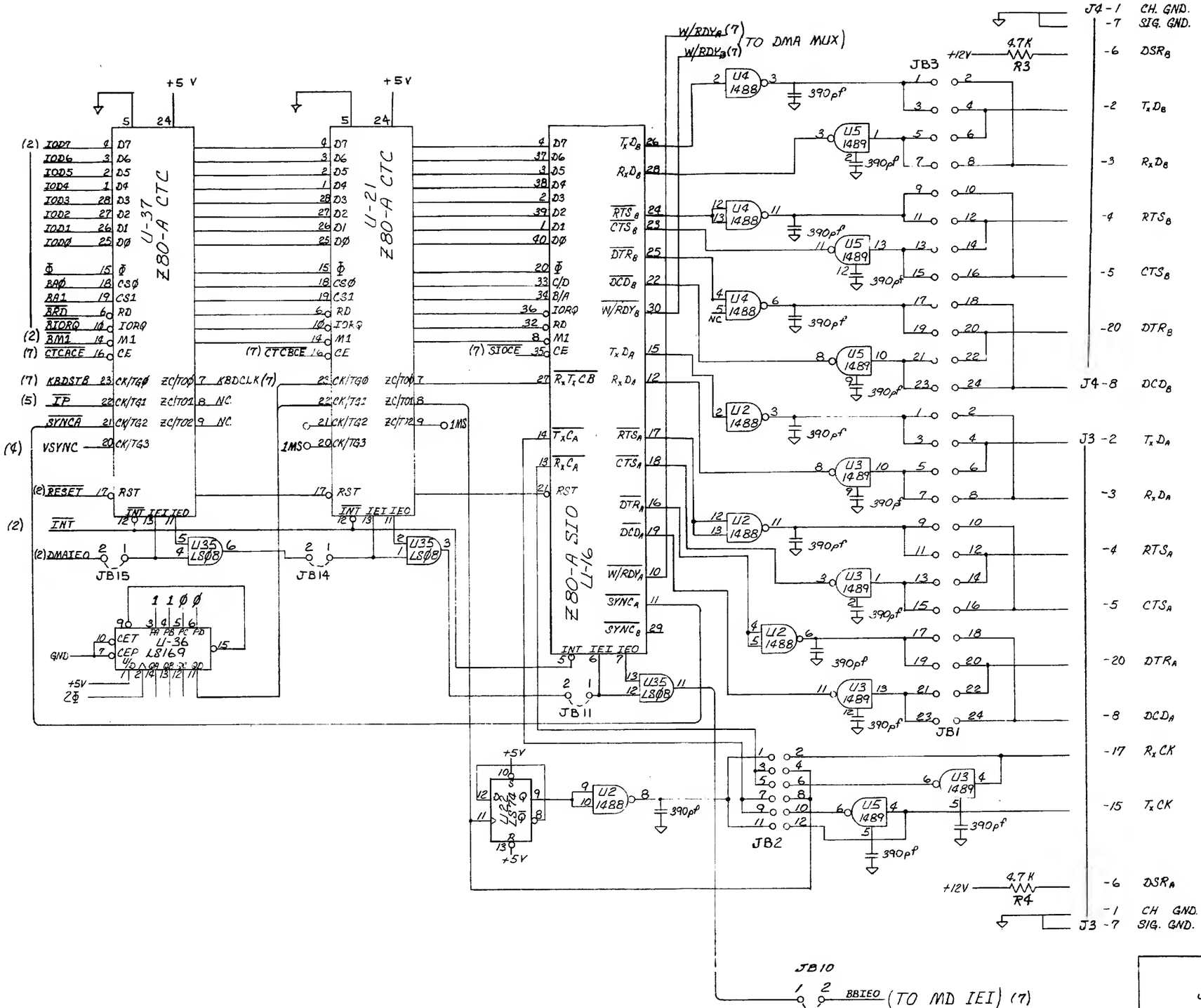
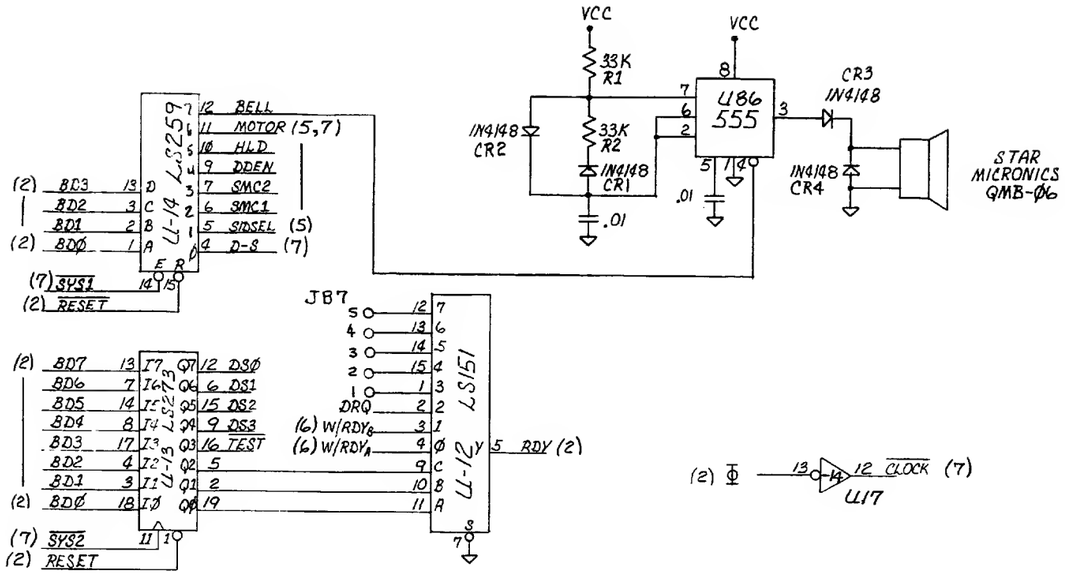
J. B. FERGUSON INC.



SERIAL I/O	
JUNE 1983	SHEET 6 OF 8
J. B. FERGUSON INC.	



STD BUS CONNECTOR - J1

COMPONENT SIDE		CIRCUIT SIDE	
+5V	1	+5V	2
GND	3	GND	4
-5V	5	-5V	6
MDD3	7	MDD7	8
MDD2	9	MDD6	10
MDD1	11	MDD5	12
MDDØ	13	MDD4	14
BAT	15	BA15	16
BA6	17	BA14	18
BA5	19	BA13	20
BA4	21	BA12	22
BA3	23	BA11	24
BA2	25	BA10	26
BA1	27	BA9	28
BAØ	29	BA8	30
MEMWR	31	MEMRD	32
BIORQ	33	MEMREQ	34
	35		36
REFSH	37		38
BM1	39		40
	41	MDBUSRQ	42
INTAK	43	INTRQ	44
WAITRQ	45	NMIRQ	46
RESET	47		48
CLOCK	49		50
	51	BBIEO	52
AUX GND	53	AUX GND	54
+12V	55	-12V	56

CONTROL

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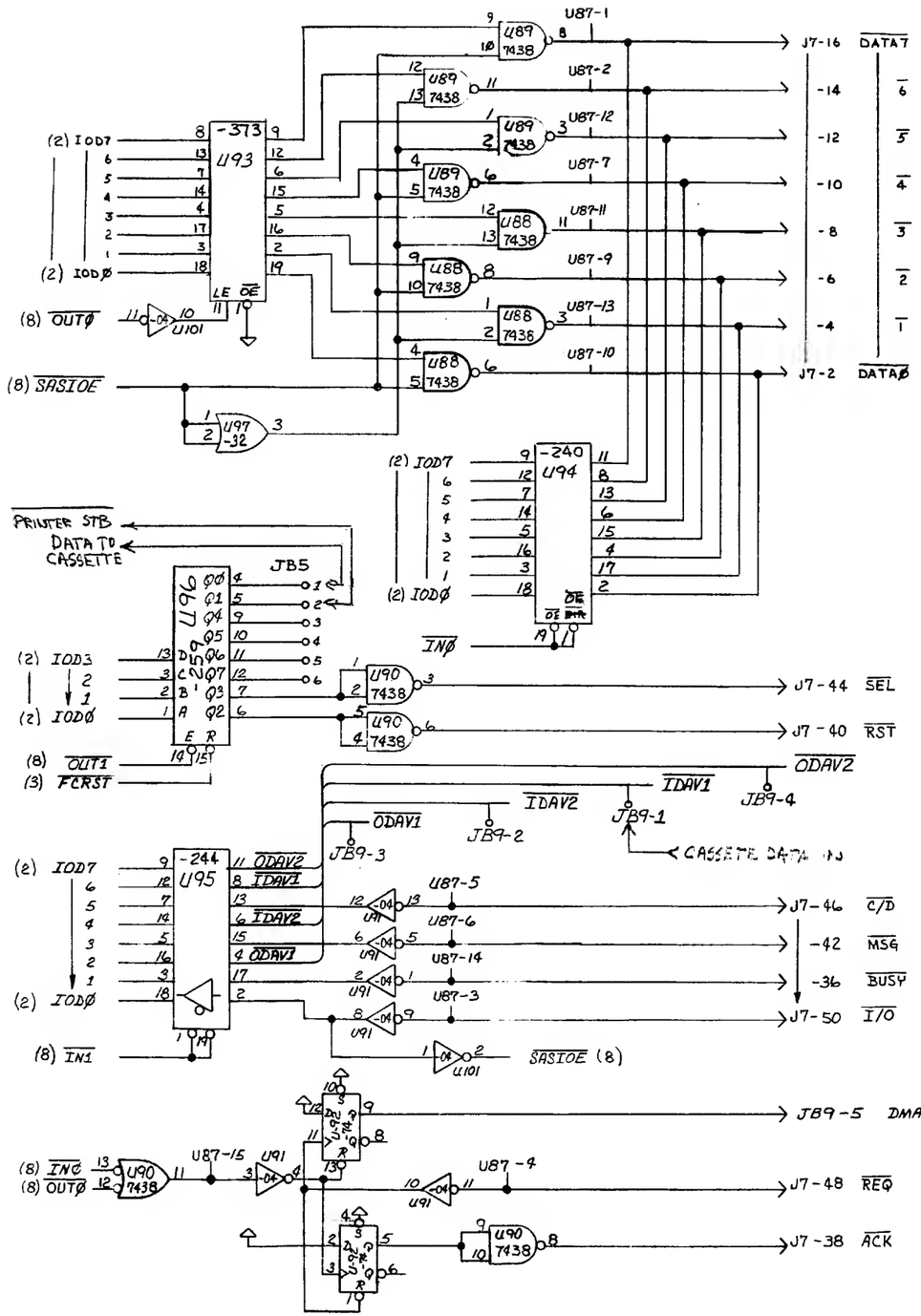
J. B. FERGUSON INC.



SASI AND PARALLEL INTERFACE

MAY 25, 1982 | SHEET 8 OF 8

J. B. FERGUSON INC.

PARALLEL KEYBOARD PORT

SERIAL PORT NO. 1

SERIAL PORT NO. 2

DISK-DRIVE CONNECTORS, ONE 50 PIN FOR 8" DRIVES, THE OTHER 34 PIN FOR 5¼" DRIVES

"SASI" INTERFACE